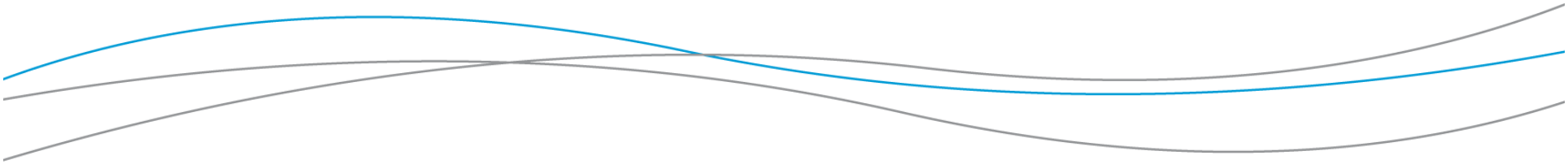


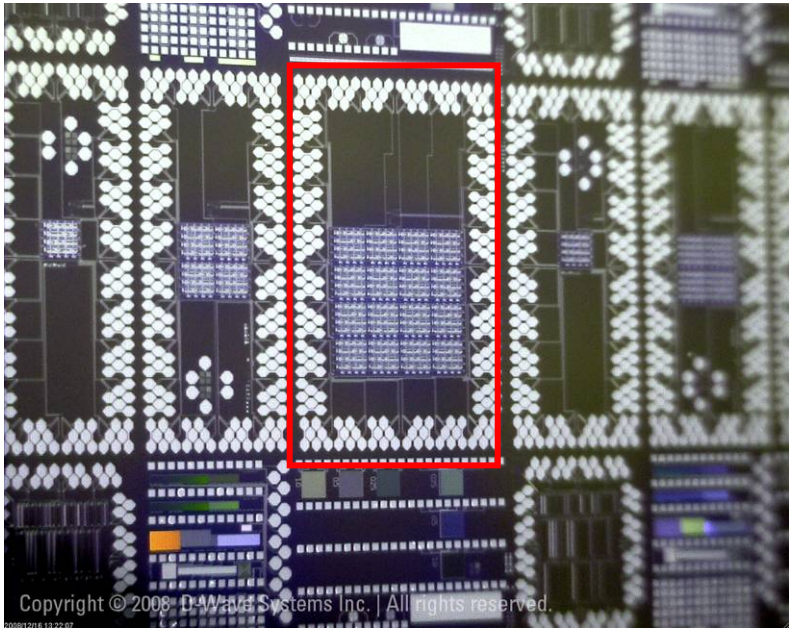
Fabrication Technology and Process Overview

January 2009

D-Wave foundry overview

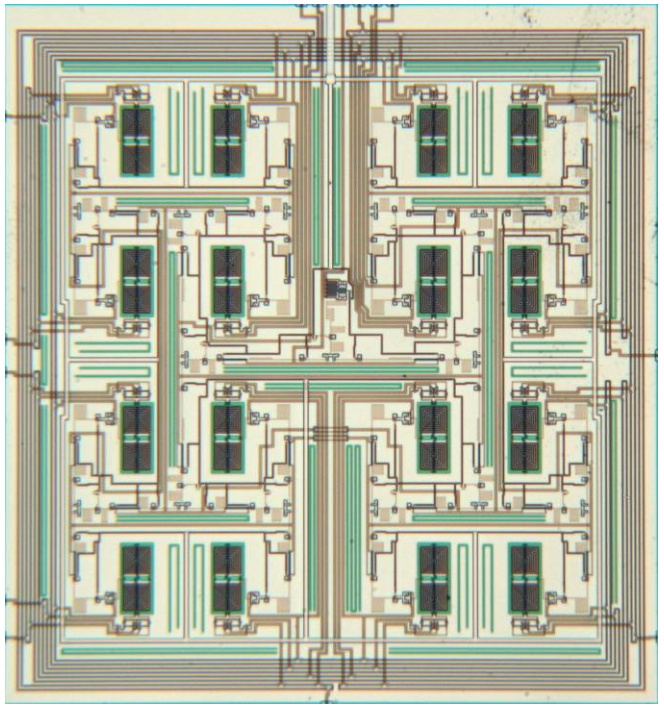
- D-Wave operates a world-class superconducting foundry, centrally managed and distributed over state-of-the-art facilities in Silicon Valley and British Columbia
- The fully planarized, sub-micron, multilayer process is realized on 200-mm wafers with throughput scalable to 10,000 to 30,000 wafers per month
- Our process utilizes industry-standard semiconductor equipment optimized for superconducting processing. The process also uses the most modern tools for in-situ metrology, continuous characterization monitoring, and operational control

Superconducting Circuit Levels of Integration



Example: SFQ-Controlled Quantum Processor

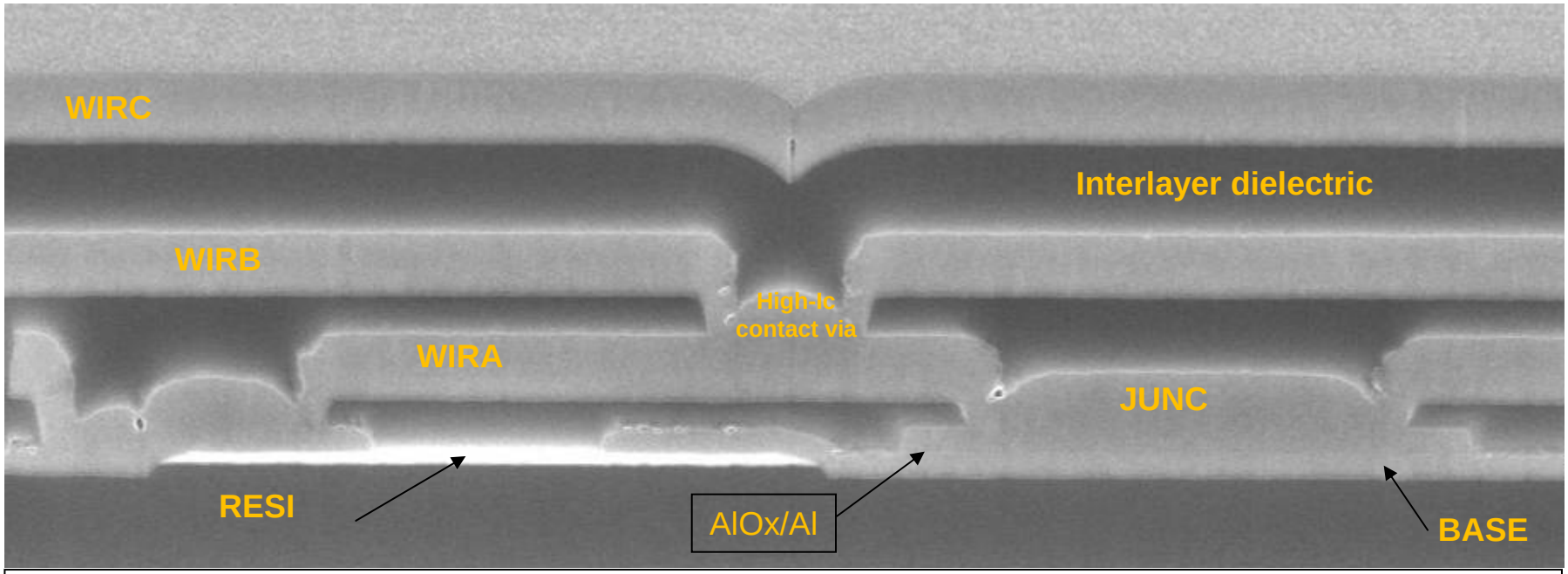
- 1,024 SFQ-based 2-stage digital to analog converters for controlling ultra-low noise analog circuitry comprising 128 quantum bits and 352 couplers
- 24,000 Josephson Junctions
- 32,000 integrated resistors



Example: Single Flux Quantum Logic

- Prototype 4-level SFQ binary de-multiplexing tree for efficient addressing
- Successfully routed 10^8 flux quanta to precise qubit inductor locations throughout test circuit without error

Fabrication Process Cross-Section

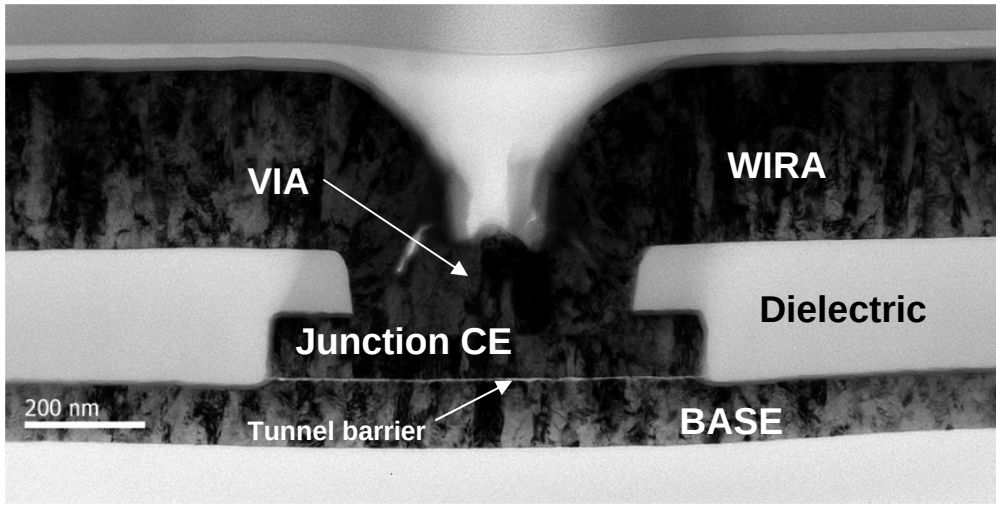


FIB cross-section of D-Wave four-metal layer process. Top dielectric layer in this circuit is not planarized.

- Sub-micron Nb-Al-AlO_x-Nb trilayer process, including junction via process for large-scale integration
- Lithography and processing enabling 0.25μm lines and spaces
- Planarized dielectric with a wide variety of materials and processes available
- Four metal wiring layers (expandable to more due to planarization of dielectric layers)
- Integrated resistors (for 4K or mK operation)

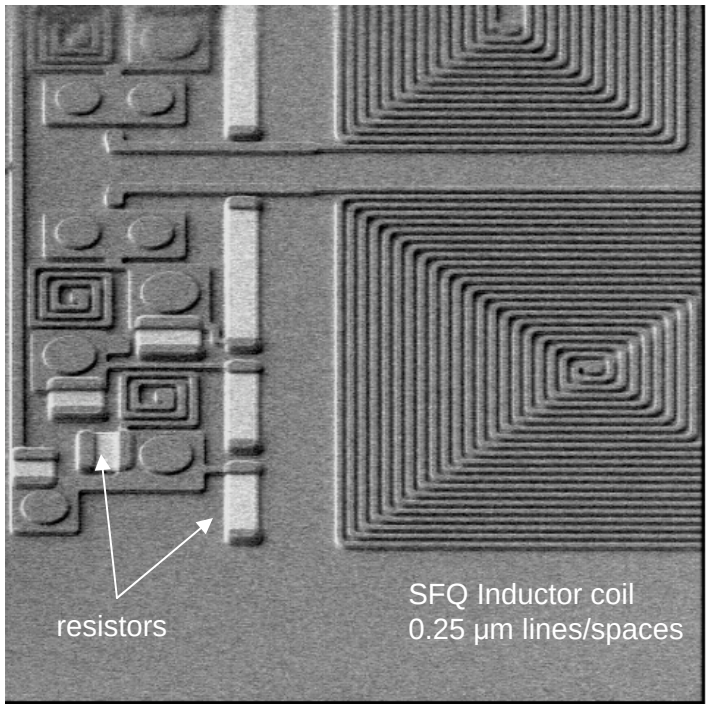
Fabrication Process Scales

TEM image of 0.6μm junction



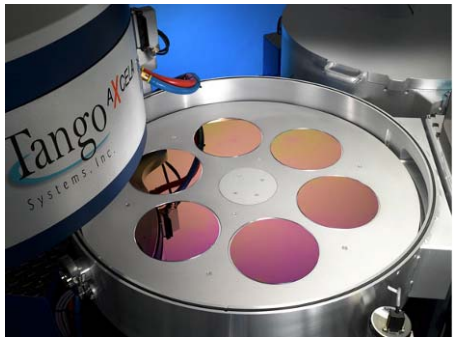
TEM illustrating VIA-to-Junction process for large-scale integration. Excellent VIA fill down to deep sub-micron scale results in high-I_c contacts between layers.

SEM image of 0.25μm wires



- Small wiring and planarization allow for very large scale integration
- Process supports quantum processor and SFQ circuits simultaneously

Key Fabrication Equipment

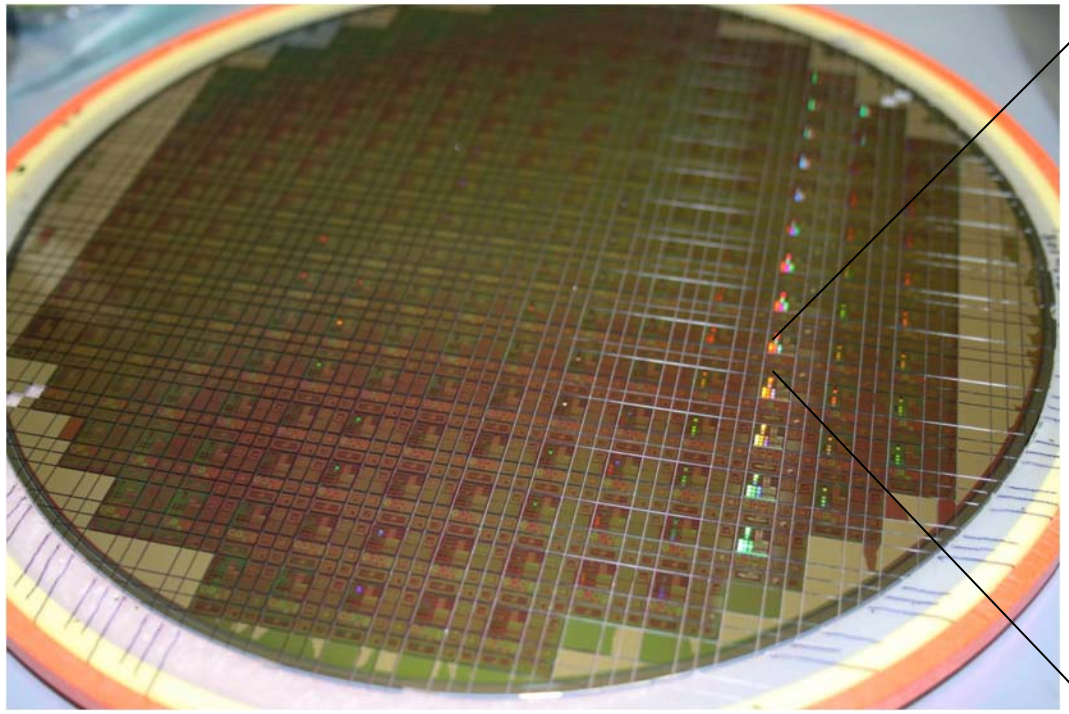


Specialized multi-chamber robotic cluster tool for high-throughput trilayer, wiring, and resistor depositions

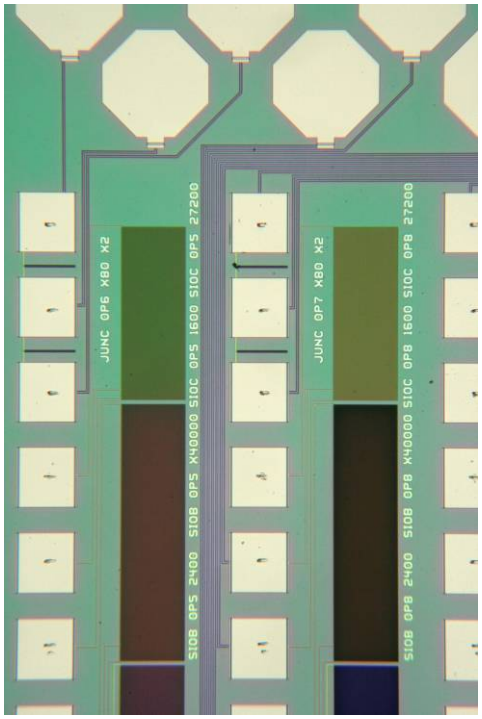
- Specialized high-throughput trilayer tooling and process
- Advanced lithography including in-situ metrology
- Wide range of low temperature PECVD and sputtered oxides
- Chemical Mechanical Polishing (CMP) on all dielectric layers for large number of wiring layers
- Full suite of analytical tools for failure analysis (FIB, SEM, TEM, AFM, etc)
- Materials characterization metrology for film optimization and noise reduction (FTIR, ellipsometry)

D-Wave

Wafer Throughput & Yield Vehicles



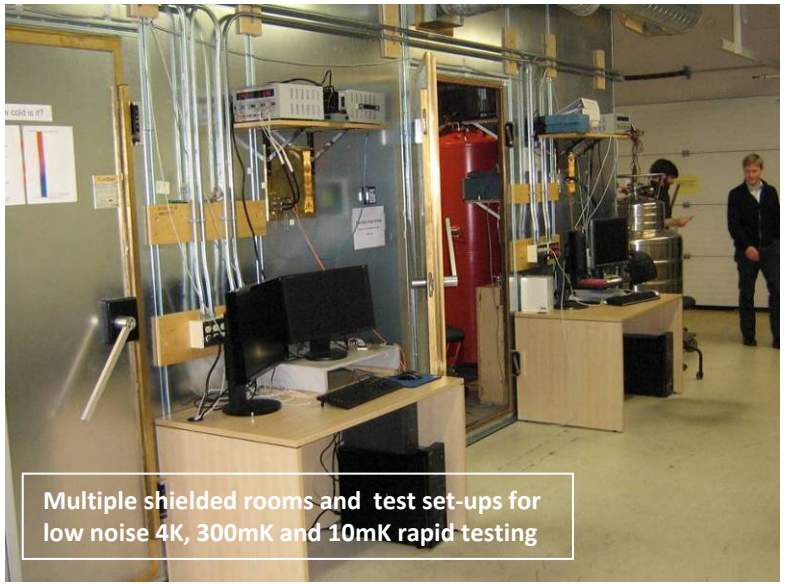
200-mm wafer containing product and process characterization dies



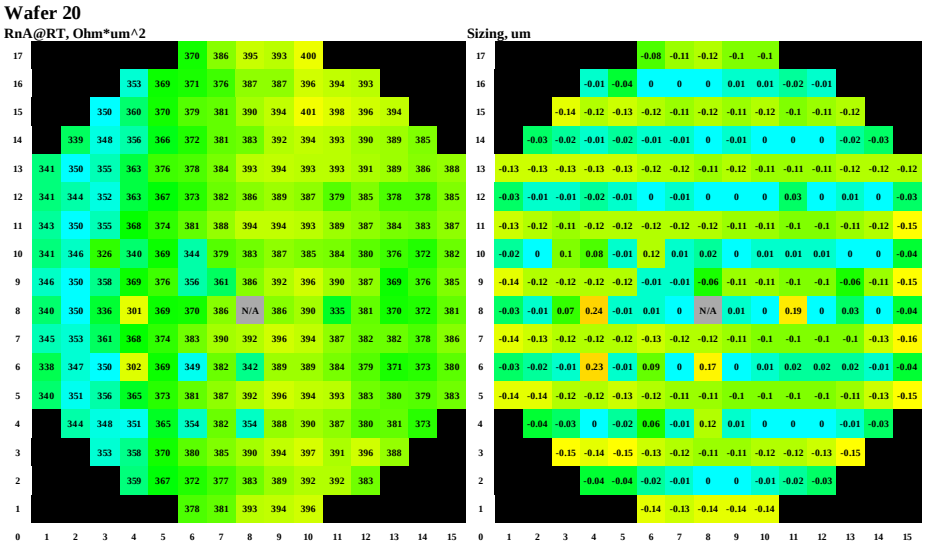
PCM chip

- Standard tooling for 200-mm wafer size
- Typically 35 wafer starts per month, expandable to manufacturing levels
- State-of-the-art commercial process tracking system incorporating electronic lot travelers, statistical process control and recipe security
- 24 hour/day, 7 days/week run schedule

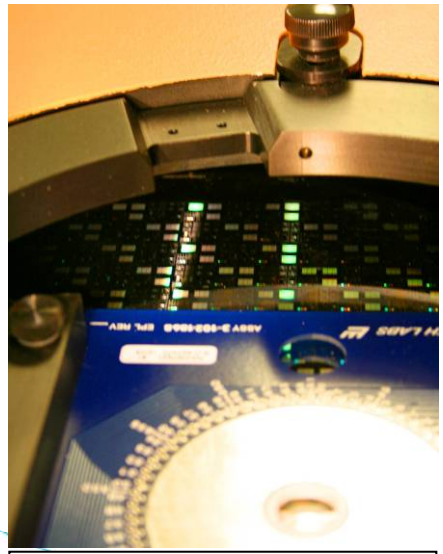
Test, Measurement, and Quality Control



Multiple shielded rooms and test set-ups for low noise 4K, 300mK and 10mK rapid testing



Wafer-level yield analysis



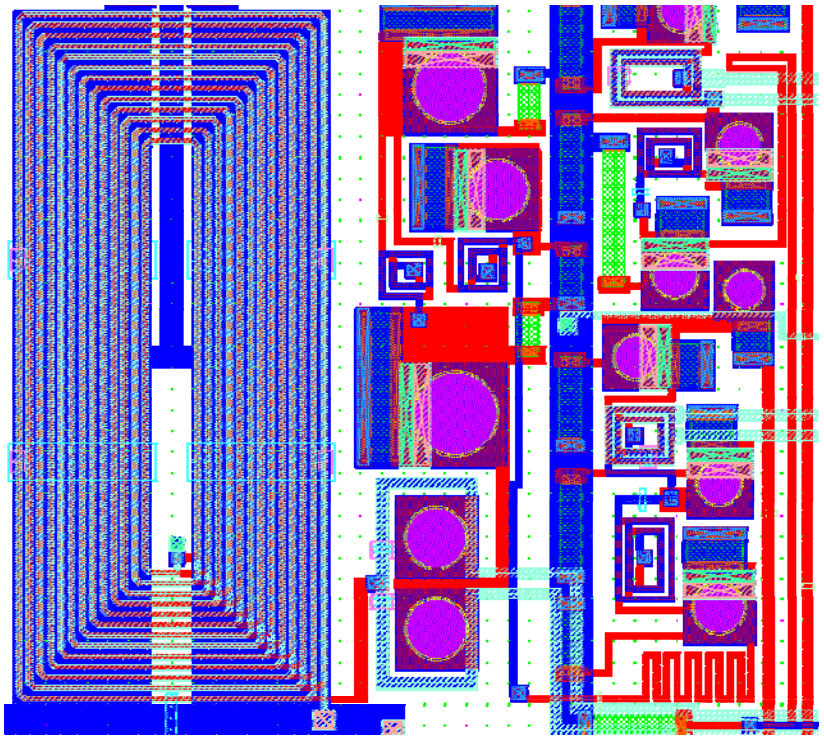
Wafer-level product chip probing

- Design knowledge and implementation of parameter characterization modules (PCM) for yield and variability monitoring and prediction
- Room temperature and cryogenic quality analysis and control
- Wafer level probing
- Noise characterization and analysis of thin films and devices
- Infrastructure enabling high-bandwidth cryogenic testing

Design and CAD Infrastructure

D-Wave Design Team is comprised of individuals who led or participated in some of the most ambitious SFQ designs to date, such as FLUX-1 microprocessor, Programmable Pass-Band Analog to Digital Converter (PBP-ADC) and Digital Signal Processor for W-CDMA Interference Cancellation.

- Design Environment
  - State of the art design capabilities within industry-standard Cadence™ Virtuoso design environment.
  - Custom interfaces to SFQ-specific circuit simulators (PSCAn, WRSpice) and inductance extraction tools (FastHenry, LMeter).
- Reference Libraries
  - Reference Libraries include Design Kit of Parameterized Cells (P-Cells) for standard circuit elements, such as Josephson junctions, resistors, inductors, capacitors, etc.
  - Design verification capabilities include complete Diva™ Design Rule Check (DRC) and Layout-vs.-Schematic (LVS) decks for our fabrication process.



CAD layout of a D-Wave digital-to-analog converter

Summary

- D-Wave has made a substantial investment and established a world-class integrated circuit fabrication infrastructure, bridging together the expertise of superconductor science and engineering with the most up-to-date industry-standard semiconductor facilities and practices
- D-Wave operations are directed towards high levels of integration and scalability, while maintaining maximum flexibility in process cross-section, materials set and tooling
- The baseline process described herein represents a foundation upon which increased metal layers and new junction targeting regimes can be easily explored
- D-Wave can significantly increase wafer throughput, and is open to expanding its fabrication capability to synergistic processes related to superconductor integrated circuit processors and applications