

D-Wave Processor Control Circuitry

Paul I. Bunyk

D-Wave Systems Inc.
Burnaby, BC Canada

- 1 Desired Hamiltonian for AQC - Review
 - What do we need control circuitry for?
- 2 D-Wave Qubit - Review
- 3 Architecture & Design
 - Chimera Architecture
 - Chip Operating Sequence
 - D-Wave Fab Process Overview
 - DAC and Demux Tree Structure & Circuits
 - DAC Requirements
- 4 Performance Validation
 - Examples of DAC control & Operating Margins
 - Requirements vs. Capabilities
 - Error Rate
 - AQO C1 Processor Operation Results

Our team – Thanks!

Design & Layout

Paul I. Bunyk
E. Tolkacheva

Testing & Analysis

Andrew J. Berkley
Mark W. Johnson
Richard Harris
Trevor Lanting
Jan Johansson

Fabrication

Eric Ladizinsky
Travis Oh

Special Thanks:

Alan Kleinsasser (JPL)
George Kerber (JPL)

and many others in Theory, Applications, I/O & Filtering, Electronics, Fridge Crew... – who made this all possible!

What are we trying to build?

Richard P. Feynman

“Simulating Physics with Computers”

International Journal of Theoretical Physics, Vol. 21, Nos. 6/7, 1982

*Can you do it [simulate Nature] with a new kind of computer – a **quantum computer**? Now it turns out, as far as I can tell, that you can simulate this with a quantum system, with quantum computer elements. It's not a Turing machine, but a machine of a different kind. [...] it does seem to be true that all the various field theories have the same kind of behavior, and can be simulated in every way, apparently, with **little latticeworks of spins and other things**.*

I will be mostly describing our “latticework” and “other things” (leaving spins to the professionals) but this is essentially what we are trying to build.

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What are we building?

Adiabatic Quantum Optimization Processor

Finding low cost solutions to a quadratic unconstrained binary optimization (QUBO) problem is equivalent to finding low energy states of the classical Ising Hamiltonian:

$$\mathcal{H} = \sum_i h_i \sigma_{zi} + \sum_{ij} J_{ij} \sigma_{zi} \sigma_{zj}$$

Adiabatic evolution to find ground and low energy states

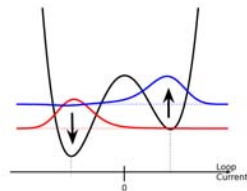
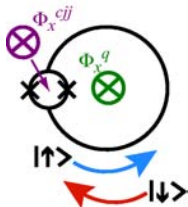
The quantum algorithm we are trying to enable is called adiabatic quantum optimization or quantum annealing, originally introduced by Farhi *et al.* The method is to adiabatically evolve a system from an initial superposition (or other) state into the ground state of desired Hamiltonian:

$$\mathcal{H} = \sum_i \Delta(t) \sigma_{xi} + \sum_i h_i \sigma_{zi} + \sum_{ij} J_{ij} \sigma_{zi} \sigma_{zj}$$

Initially $\Delta(0) \gg h_i, J_{ij}$, finally $\Delta(t_f) = 0$, somewhere along the way where $\Delta \approx h_i, J_{ij}$ “quantum magic” happens!

Desired Hamiltonian

$$\mathcal{H} = \sum_i \Delta(t) \sigma_{xi} + \sum_i h_i \sigma_{zi} + \sum_{ij} J_{ij} \sigma_{zi} \sigma_{zj}$$



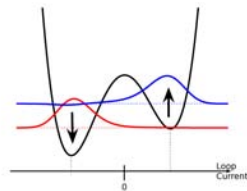
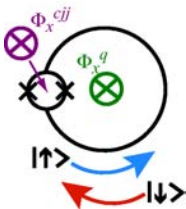
Flux qubits Hamiltonian

$$\mathcal{H} = \sum_i \Delta(\Phi_{xi}^{cjj}) \sigma_{xi} + \sum_i \Phi_{xi}^q I_{pi} (\Phi_{xi}^{cjj}) \sigma_{zi} + \sum_{ij} M_{ij} \cdot I_{pi} (\Phi_{xi}^{cjj}) I_{pj} (\Phi_{xi}^{cjj}) \sigma_{zi} \sigma_{zj}$$

Can be mapped onto each other...

Desired Hamiltonian

$$\mathcal{H} = \sum_i \Delta(t) \sigma_{xi} + \sum_i h_i \sigma_{zi} + \sum_{ij} J_{ij} \sigma_{zi} \sigma_{zj}$$



Flux qubits Hamiltonian

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Can be mapped onto each other... But what else do we need to make “quantum magic” happen? **Need to make all physical qubits identical!**

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D-Wave Qubit – Variant of rf SQUID flux qubit

Tunable Compound junction

→ Controls tunnel splitting

Tunable Couplers

→ Configure Ising Hamiltonian J_{ij}

Inductance Tuner

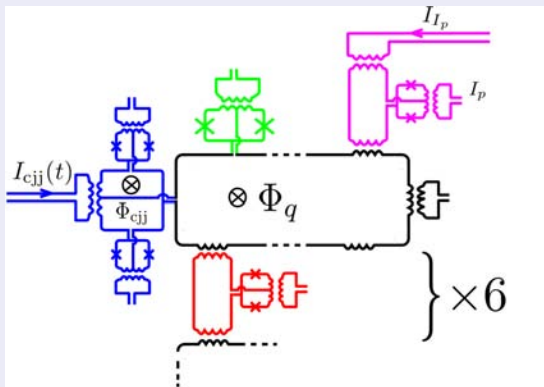
→ Remove effects of coupler loading

Compound/Compound junction

→ Remove junction asymmetry
and inter-qubit variability

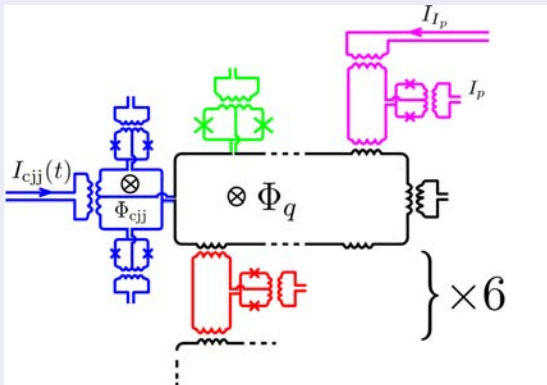
Gain tunable flux bias transformer

→ Apply Ising Hamiltonian $h_i(I_{pi}(t))$



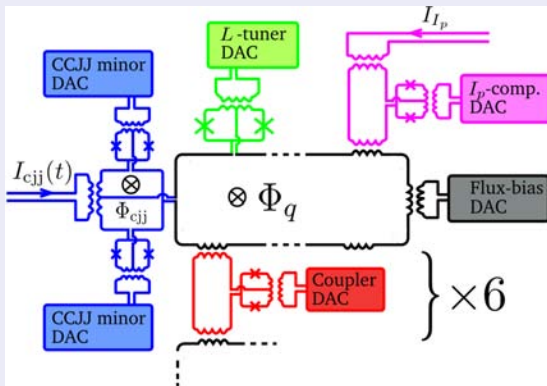
D-Wave Qubit – Variant of rf SQUID flux qubit

- Five control *knobs* per qubit
- Another for each coupler
- About 1000 *filtered* Wires to mK for 128 Qubits! → **Too Many Wires!**
- Need addressable on-chip digital-to-analog flux converters (DACs) and SFQ demultiplexors to address them.



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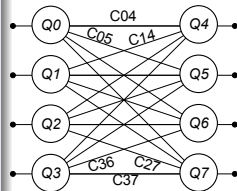
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Processor topology

To a Theorist:

- Qubit is an individual spin, a *dot*, node in a graph.
- Coupler is a line between dots. Would prefer a complete graph, but would take something into which complete graphs can be *embedded*.
- Should at least be non-planar (makes Ising spin problems NP-hard).
- *E.g.*, $K_{4,4}$ Bipartite graph



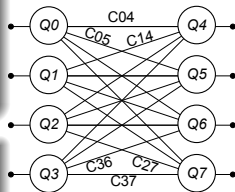
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In practice:

- Our flux qubits are large β_L SQUIDs (long), couplers are smaller β_L SQUIDs (shorter).
- Qubits can be stretched and bent as needed!
- Unit cell of what we call *Chimera topology* (C1), physical implementation of $K_{4,4}$ Bipartite graph



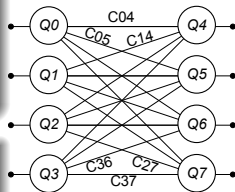
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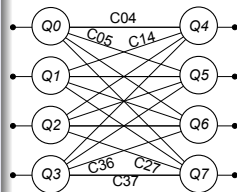
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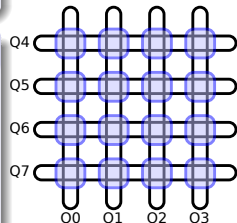
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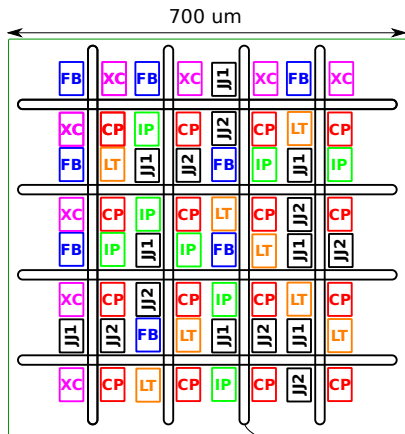
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D:WAVE
The Quantum Computing Company™

C1 Block Diagram: 8 qubits, 64 DACs



FB - Qubit Flux Bias DAC

JJ1,2 - Compound/compound Junctions and DACs

IP - Circulating current compensation DAC

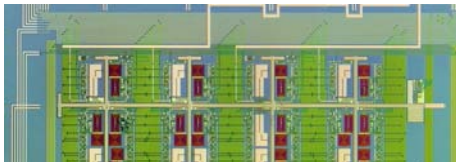
LT - L-Tuner DAC

CP - Coupler DAC

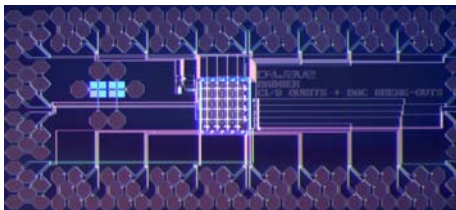
XC - Inter-Block Coupler DAC

Qubit Inductor

- Top-most qubit with DACs and wiring channels visible



- Individual C1 test chip



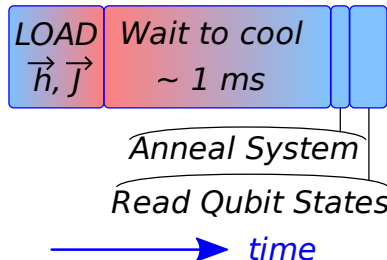
Chip Operating Sequence

Sequential program and anneal steps

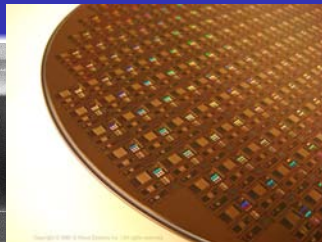
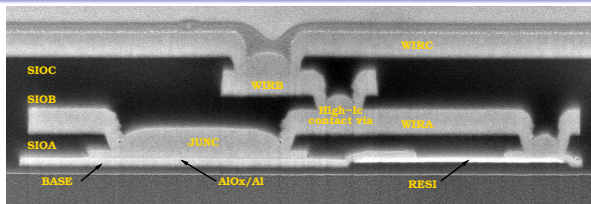
Step	Approx. Time
Load \vec{h}, \vec{J}	100 μs
Wait to cool	1 ms
Anneal system	10 μs
Read qubit state	100 μs

- Powering up demux generates heat
- Loading DACs raises chip temperature to about 400 mK
- Wait to cool off before annealing

Chip Level Timing Diagram



Fabrication process overview



D-Wave Fab

- 8" wafers, in 12-24 wafer lots
- 4-6 week turnaround
- Nb/Al/AIO_x/Nb junctions
- Four Nb wiring layers
- TiPt resistive layer
- Planarized SiO₂ dielectric

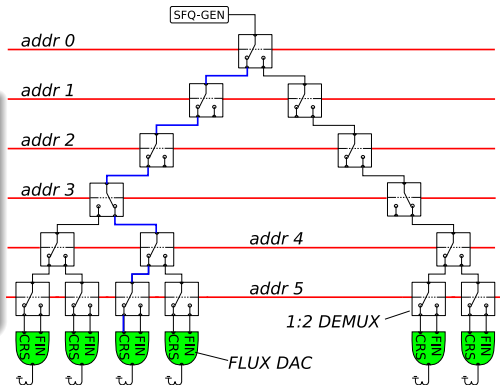
Some design rules

- 0.25 μm lines and spaces (DAC spirals!)
- 0.6 μm minimum diameter junction
- 10 mA/ μm^2 via critical current

Closer look at DACs and demuxes

Digital to analog converters

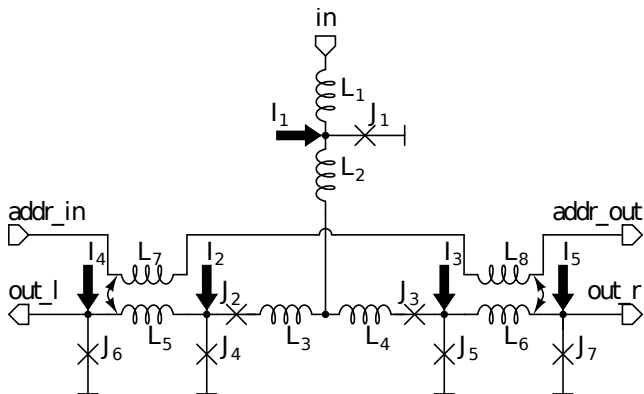
- Set qubit/chip size!
- Addressed by demultiplexer tree
- Two large ($\sim 2nHn$) flux storage inductors loaded by SFQ pulses



Demultiplexer tree

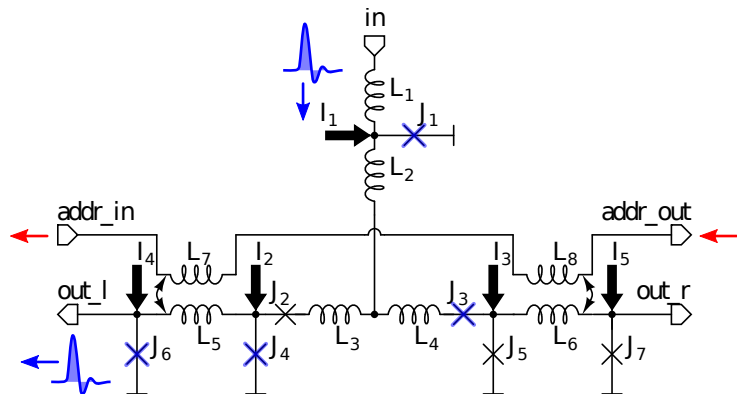
- Route pulses to proper DAC.
- Dissipates power during loading, none while quiescent.
- Very simple (by design!) SFQ circuit.

1:2 Demultiplexer Gate



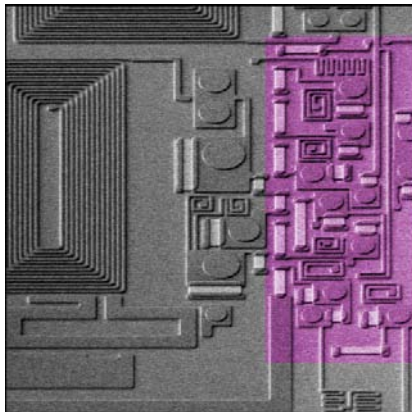
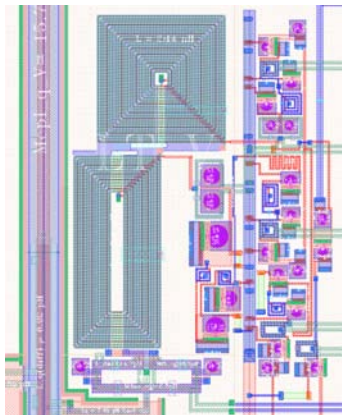
- Magnetically coupled address line steers incoming SFQ pulses ...
- Φ_0 to left ... ($-\Phi_0$ with power & address sign change)
- Φ_0 to the right ...

1:2 Demultiplexer Gate



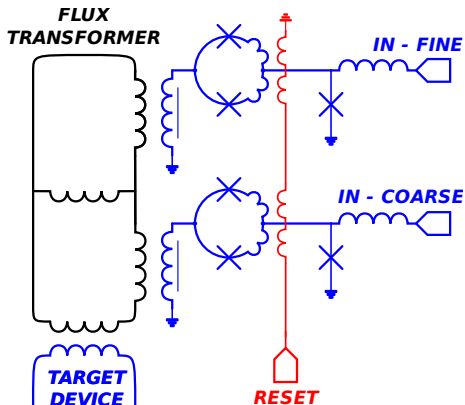
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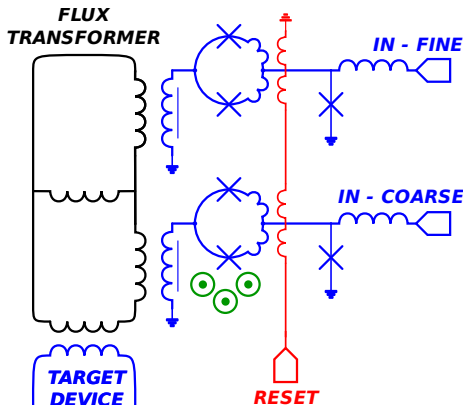
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Two Stage DAC



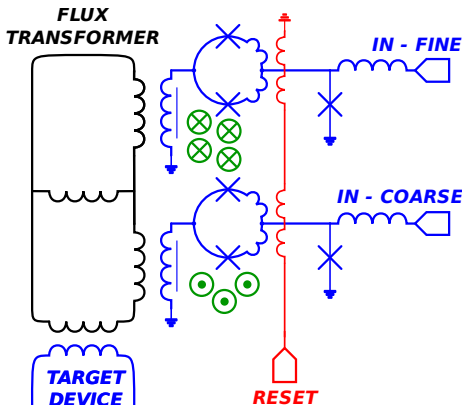
- Each flux storage loop contains small (< 40) integer number of Φ_0
- $+3\Phi_0$ in the COARSE loop
- $-4\Phi_0$ in the FINE loop
- Flux Coupled Out = $k \cdot (N_{\text{COARSE}}\Phi_0 + \gamma \cdot N_{\text{FINE}}\Phi_0)$
with γ typically chosen $\simeq 0.1$

Two Stage DAC



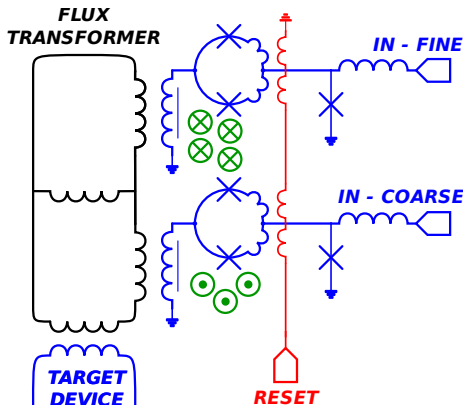
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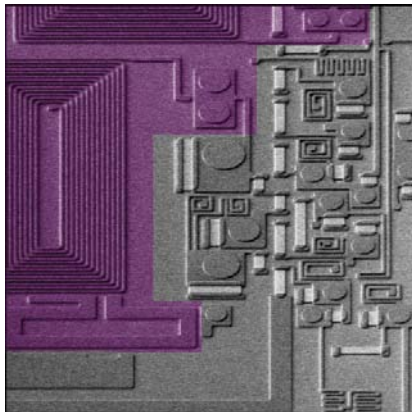
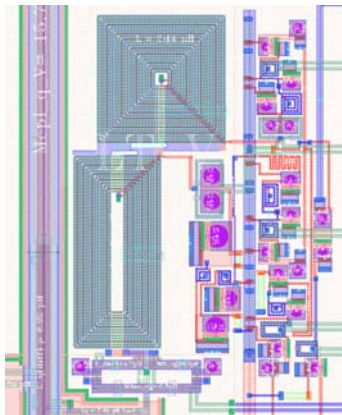
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Two Stage DAC



- Coils are tens of turns at $0.25 \mu\text{m}$ lines & spaces each.
- Signal pick-up washers are not trivial to design at all!
- Succeeded using advanced FastHenry interface.

Different DAC flavors (and Challenges)

- DACs used for different purposes have to have different ranges
 - Some need to provide almost a full Φ_0 swing into its target device!
- All DACs have to have about 8 effective bits of precision (BOP)
 - To achieve 4 BOP in QUBO specification, taking target device non-linearity into account.

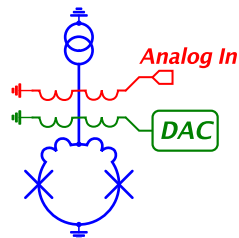
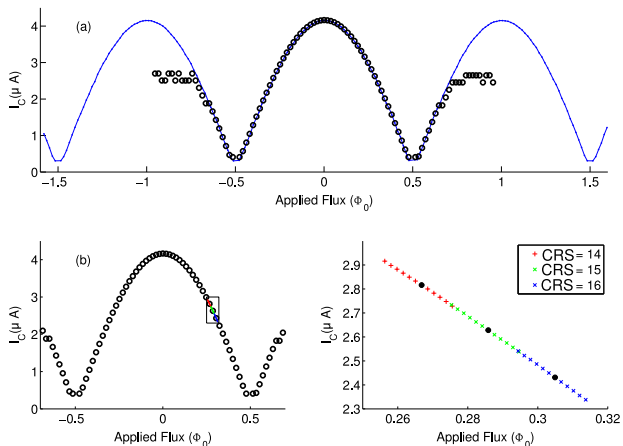
Designed flux ranges and minimal flux steps by DAC type

DAC Type	Span	min $\Delta\Phi$	Maximum #		1/ γ
			COARSE	FINE	
Qubit Flux Bias	25.5 $m\Phi_0$	0.1 $m\Phi_0$	17	17	14.1
CJJ Balancing	66.1 $m\Phi_0$	0.4 $m\Phi_0$	17	17	14.1
L-Tuner	0.465 Φ_0	1.1 $m\Phi_0$	40	10	10.7
Coupler/ I_P -comp.	0.968 Φ_0	2.2 $m\Phi_0$	40	10	10.6

Outline

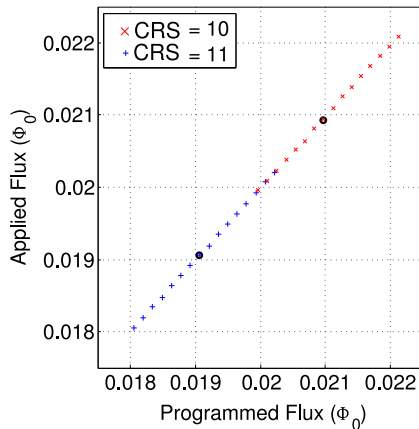
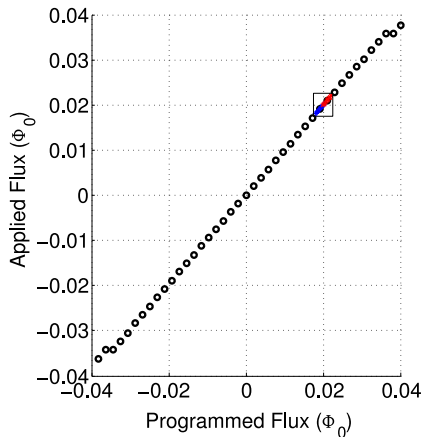
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DAC vs. analog control line flux-biasing a dc-SQUID



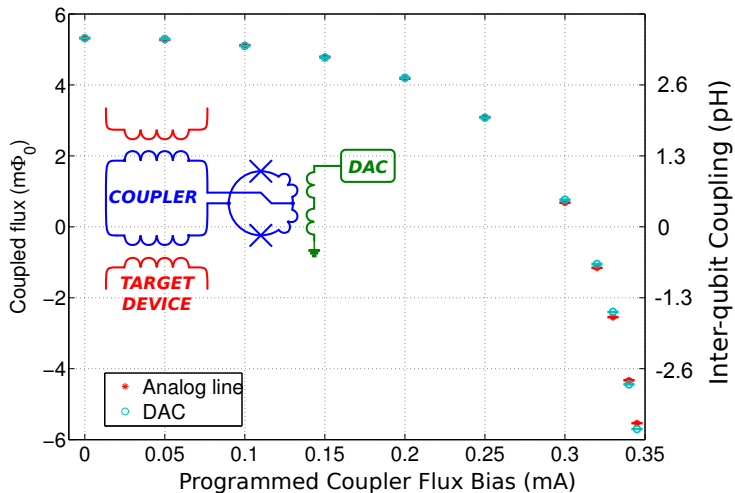
- Achieved $> \Phi_0$ range into a small β ($\ll 1$) dc-SQUID
- FINE range spans COARSE step size
- $\gtrsim 290$ levels, or more than 8 bits

Qubit Flux Bias DAC

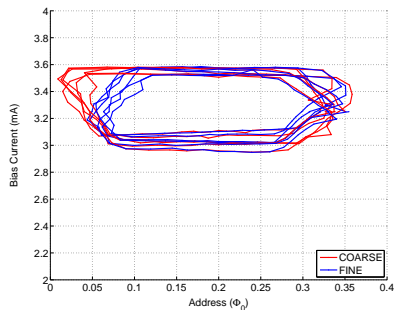
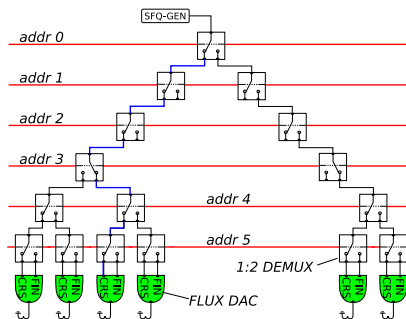


- Full scale range $\pm 30m\Phi_0$
- FINE range spans COARSE step size

Programmable Qubit/Qubit Coupling

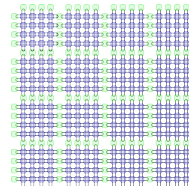
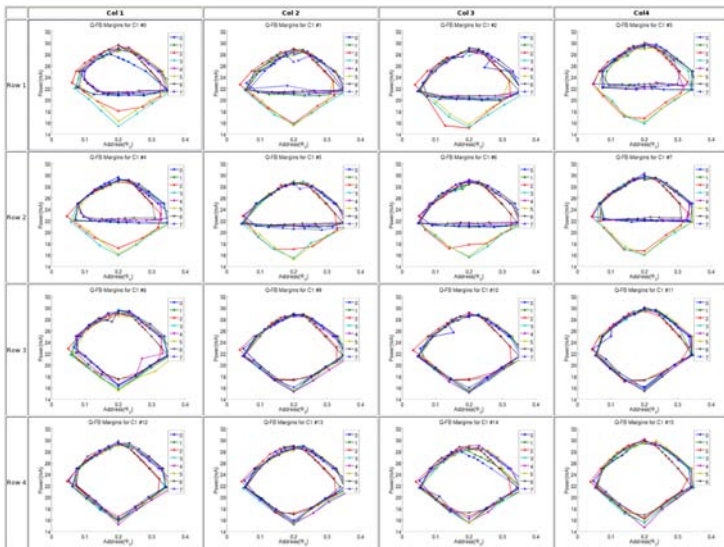


Operating Margins



- Power/address operating margins to route to 8 X-Coupler DACs
- A Common power and address level works for all devices on chip

Operating Margins - 128 Qubit Flux Bias DACs, 24,000 JJ



DAC Designed vs. Achieved – FastHenry was right!

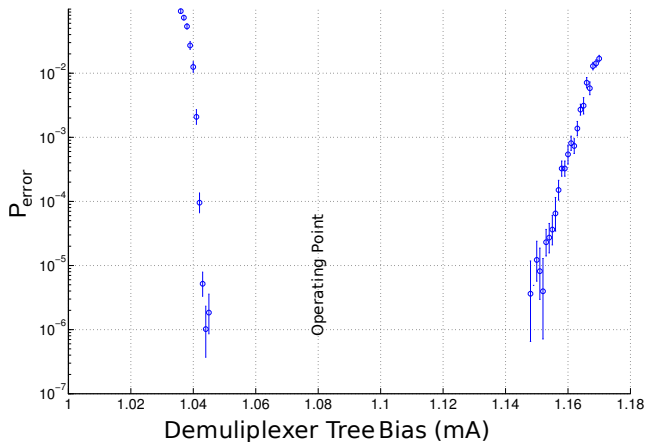
COARSE and FINE DAC step weights

DAC Type	COARSE Step ($m\Phi_0$)		FINE Step ($m\Phi_0$)	
	Design	Achieved	Design	Achieved
Qubit Flux	3.0	3.506 ± 0.003	0.21	0.268 ± 0.003
CJJ Balance	5.6	3.899 ± 0.002	0.40	0.296 ± 0.003
L-Tuner	11.3	8.481 ± 0.001	1.1	1.061 ± 0.001
Coupler	23.6	19.0221 ± 0.0002	2.2	1.788 ± 0.001

Maximum storage capacity, maximum applied flux

DAC Type	MAX COARSE Φ_0		Max Coupled Flux (Φ_0)	
	Designed	Achieved	Designed	Achieved
Qubit Flux	17	22	0.050	0.077
CJJ Balance	17	22	0.093	0.086
L-Tuner	41	40	0.460	0.339
Coupler	41	35	0.960	0.665

The Probability of Making a Programming Error



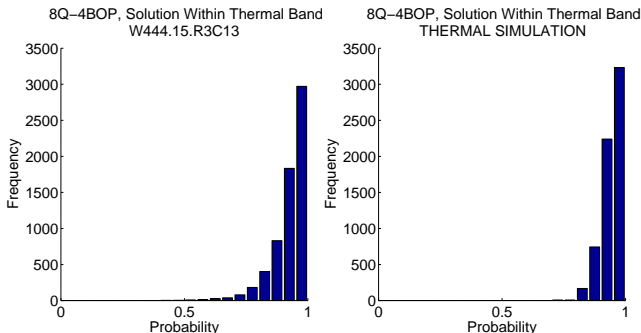
- At Operating Point: No errors in 15,300,000 operations
→ 95% confidence $P_{\text{error}} < 2.5 \times 10^{-7}$
- Exclusivity

C1 AQO processor operation under DAC control

Low Energy Solutions

The hardware returns low energy solutions with very high probability. This is the expected behaviour of a AQO processor operated at finite T.

Success histograms over 6400 unique problems, each run 1024 times



More details are available on arXiv

- Qubit** *Experimental Demonstration of a Robust and Scalable Flux Qubit*
R. Harris, J. Johansson, A.J. Berkley, M. W. Johnson, T. Lanting, Siyuan Han, P. Bunyk, E. Ladizinsky, T. Oh, I. Perminov, E. Tolkacheva, S. Uchaikin, E. Chapple, C. Enderud, C. Rich, M. Thom, J. Wang, B. Wilson, G. Rose
arXiv:0909.4321
- Coupler** *A Compound Josephson Junction Coupler for Flux Qubits With Minimal Crosstalk*
R. Harris, T. Lanting, A.J. Berkley, J. Johansson, M. W. Johnson, P. Bunyk, E. Ladizinsky, N. Ladizinsky, T. Oh, Siyuan Han
arXiv:0904.3784
- PCC** *A scalable control system for a superconducting adiabatic quantum optimization processor*
M. W. Johnson, P. Bunyk, F. Maibaum, E. Tolkacheva, A. J. Berkley, E. M. Chapple, R. Harris, J. Johansson, T. Lanting, I. Perminov, E. Ladizinsky, T. Oh, G. Rose
arXiv:0907.3757
- Read-out** *A scalable readout system for a superconducting adiabatic quantum optimization system*
A. J. Berkley, M. W. Johnson, P. Bunyk, R. Harris, J. Johansson, T. Lanting, E. Ladizinsky, E. Tolkacheva, M. H. S. Amin, G. Rose
arXiv:0904.3784
- Noise** *Geometrical dependence of low frequency noise in superconducting flux qubits*
T. Lanting, A.J. Berkley, B. Bumble, P. Bunyk, A. Fung, J. Johansson, A. Kaul, A. Kleinsasser, E. Ladizinsky, F. Maibaum, R. Harris, M. W. Johnson, E. Tolkacheva, M.H.S. Amin
Phys. Rev. B 79 060509 (2009) and arXiv:0812.0378

Conclusions

- Implemented SFQ Programmable Control Circuitry for AQO Processor
- On the first attempt at our current mask (Rainier)!
With 3 subsequent performance-enhancing revisions...
- Characterized a few each of
 - 8 qubit 64 DAC 1500 JJ (C1) chips
 - 128 qubit 992 DAC 24,000 JJ (C4) chips
- Behaves largely as expected - meets requirements!
- Failures are mostly parametric – this is an analog system, redundant by design! Ignoring qubits with, say, $> 3\%$ asymmetry.
- Used to obtain most recent C1 Processor results
- Thermally distributed results, consistent with *complete system being quantum!* More analysis needed, but it looks that it would behave differently if it were purely classical.
- Three C4 processor chips are currently being calibrated.
- Stay tuned!

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